5. (Amended) A method for fabricating a shallow-trench isolation transistor on a semi-conductor substrate including:

forming a single isolation trench having a uniform cross section to define an active region in the silicon substrate;

performing sidewall isolation implants on the side and bottom walls of said isolation trench;

depositing a dielectric isolation material in said isolation trench;

planarizing the top surface of said silicon substrate and said dielectric isolation material;

forming a gate oxide layer over said active region in said silicon substrate;

forming and defining gate regions over said oxide layer in said active region in said silicon substrate; and

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forming source and drain regions in the active region in the silicon substrate.

6. (Amended) The method of claim 5 wherein performing said sidewall implants comprises implanting p-type impurities.

7. (Amended) The method of claim 6 wherein implanting p-type impurities comprises implanting boron.

8. (Amended) The method of claim 6 wherein implanting p-type impurities comprises implanting boron to a concentration of about 2e12.